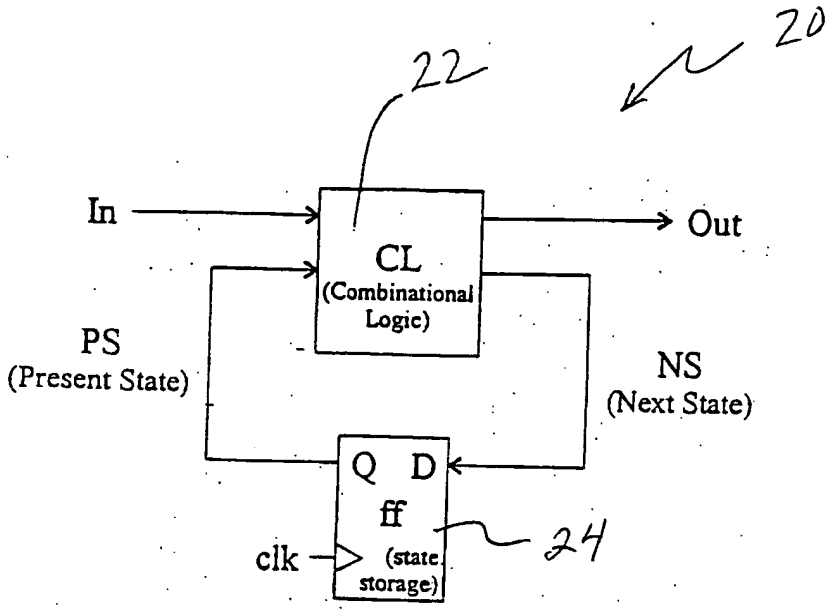

20
22
In
Out
CL
(Combinational
Logic)
PS
(Present State)
NS
(Next State)
Q D
ff
clk
(state
storage)
24

FIG. 1

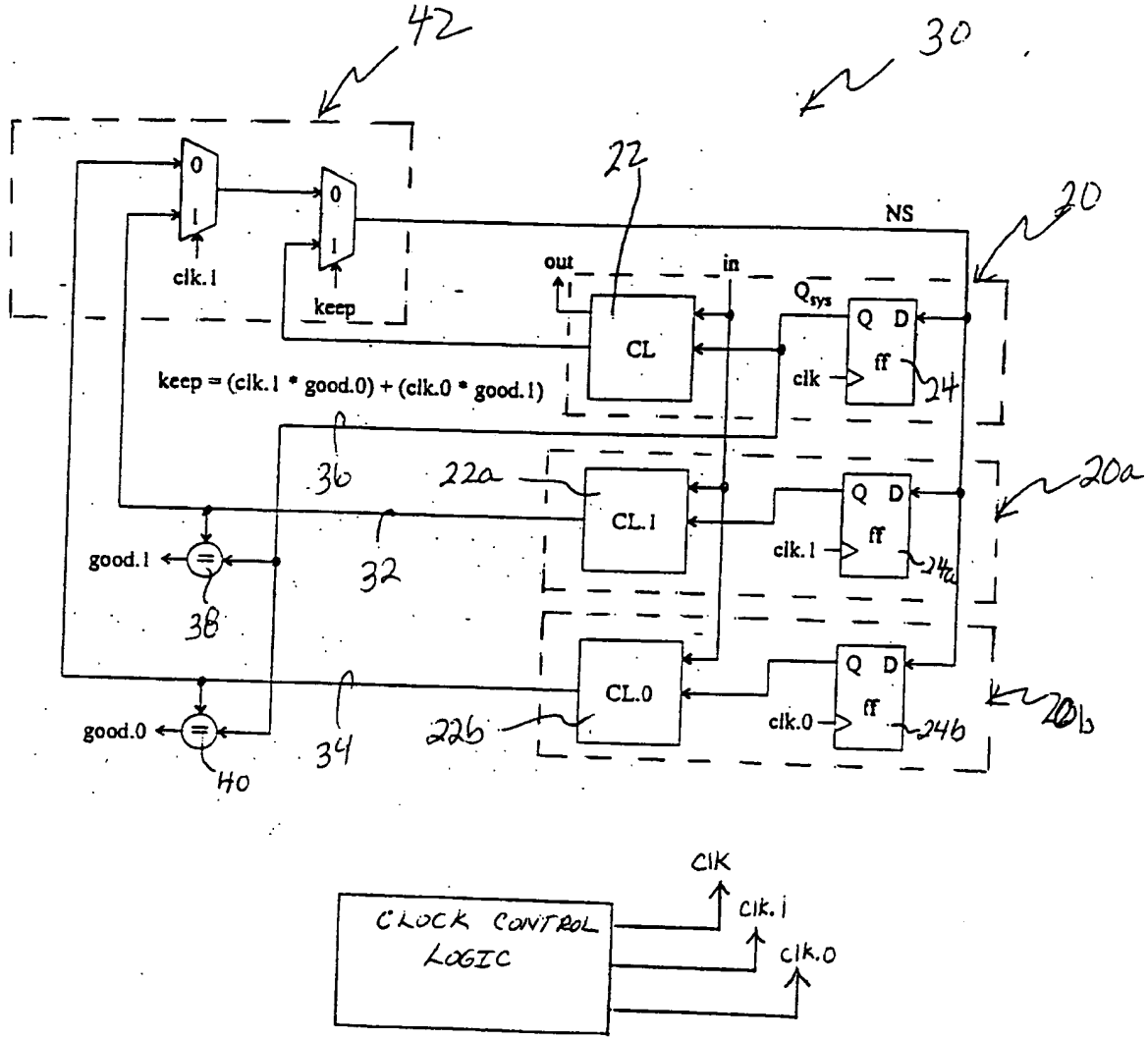

42
30
22
20
NS
0
1
clk.1
keep
out
in
Q_{sys}
Q D
ff
CL
clk
24
keep = (clk.1 * good.0) + (clk.0 * good.1)
36
22a
CL.1
20a
good.1
32
38
clk.1
24a
CL.0
20b
good.0
34
22b
40
clk.0
24b
CLOCK CONTROL LOGIC
CLK
clk.1
clk.0

FIG. 2

URI.5077

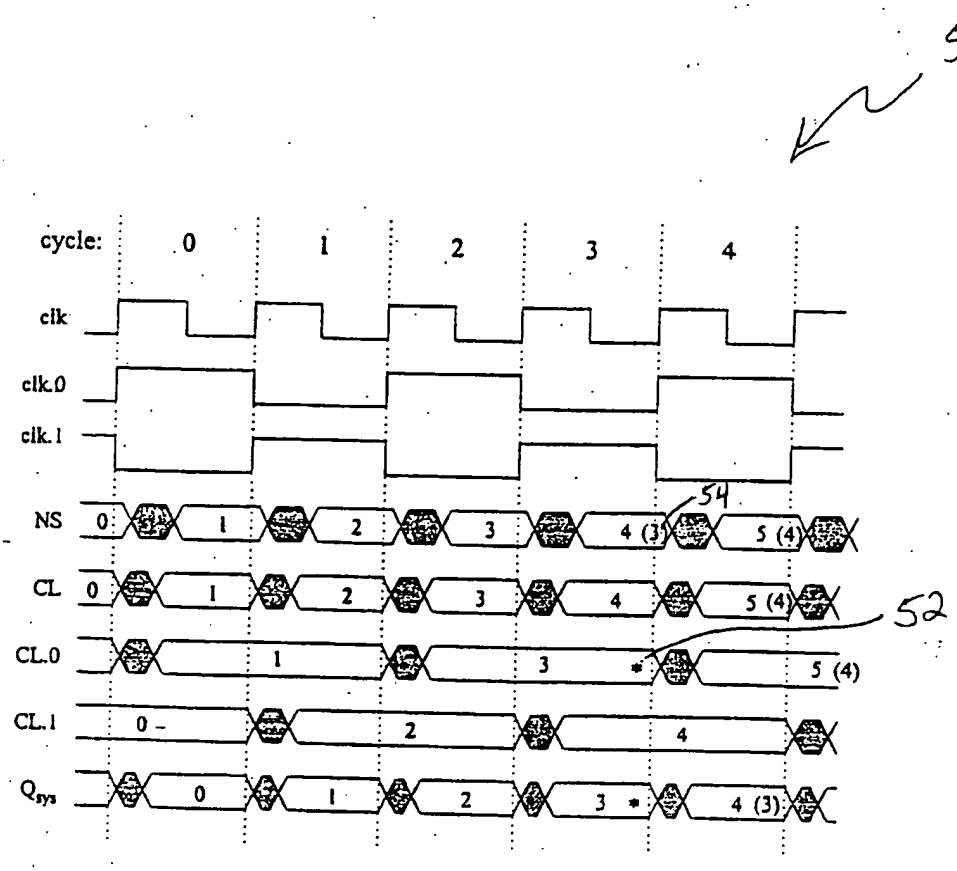
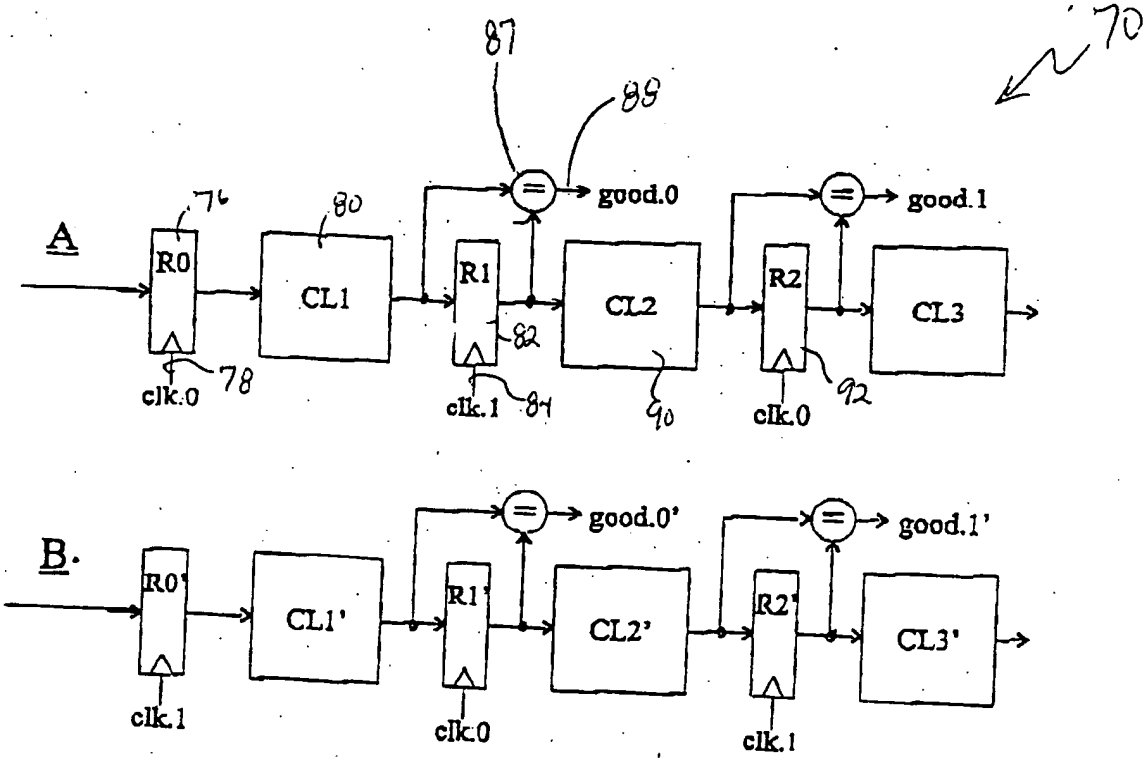


FIG. 3


70
87
89
A
R0
76
CL1
80
R1
CL2
R2
CL3
good.0
good.1
clk.0
78
clk.1
82
84
90
clk.0
92
B.
R0'
CL1'
R1'
CL2'
R2'
CL3'
good.0'
good.1'
clk.1
clk.0
clk.1

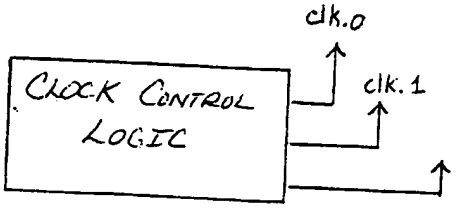

clk.0
CLOCK CONTROL LOGIC
clk.1

FIG. 4

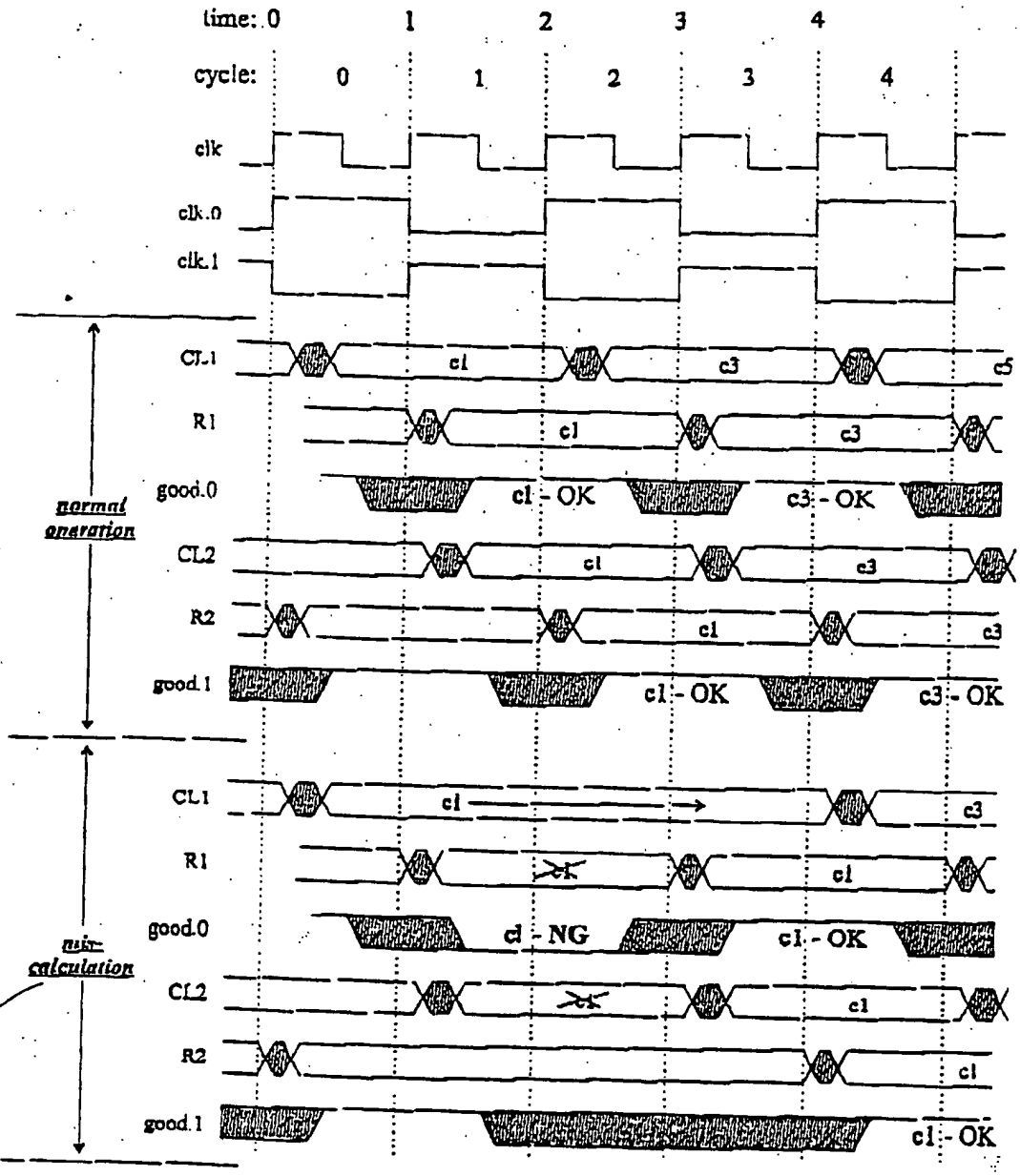

time: 0
1
2
3
4
cycle:
0
1
2
3
4
clk
clk.0
clk.1
CL1
c1
c3
c5
R1
c1
c3
good.0
c1 - OK
c3 - OK
normal operation
CL2
c1
c3
R2
c1
c3
good.1
c1 - OK
c3 - OK
CL1
c1
c3
R1
c1
good.0
c1 - NG
c1 - OK
mis-calculation
CL2
c1
R2
c1
good.1
c1 - OK
94

FIG. 5

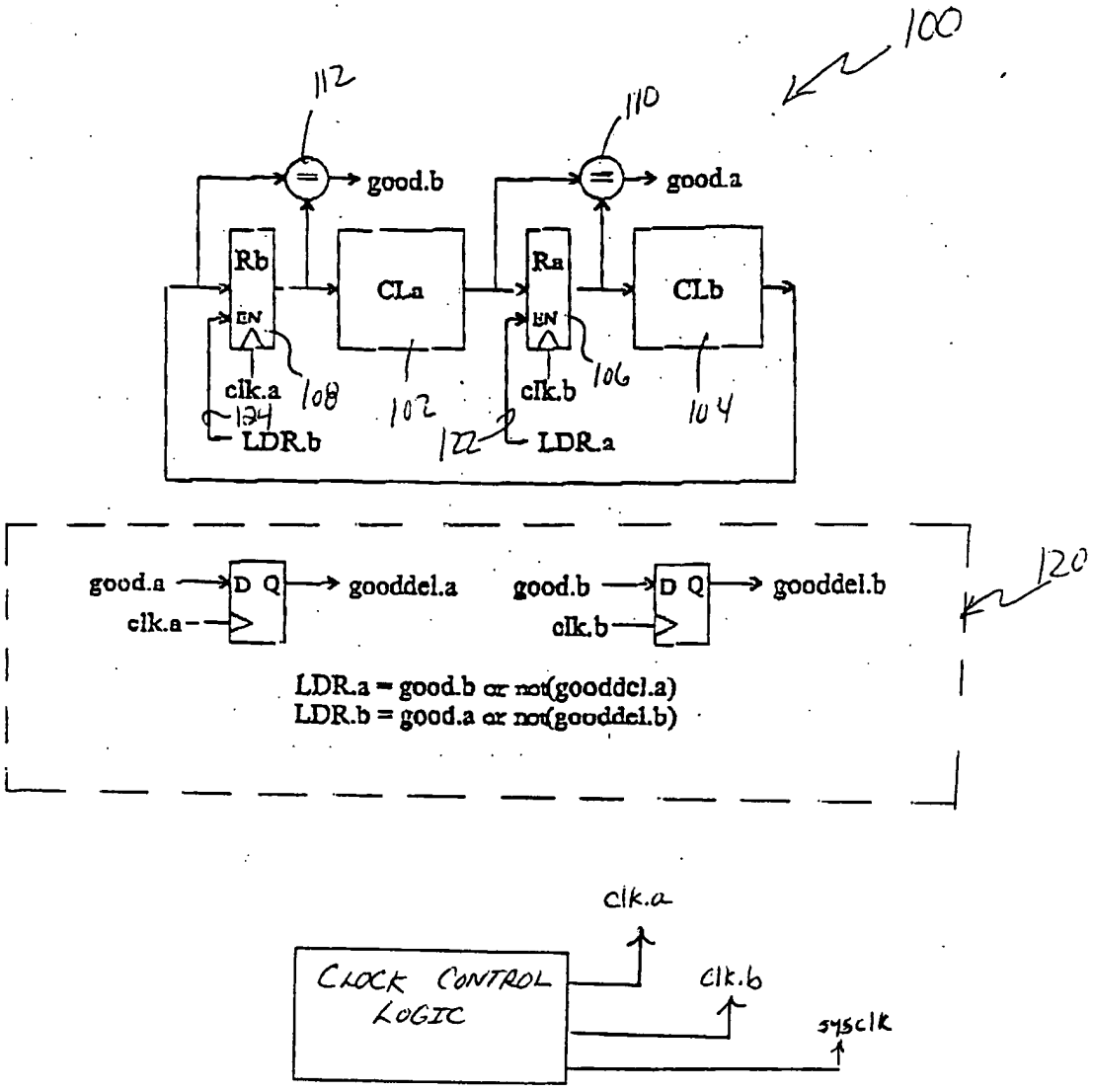

100
112
110
good.b
good.a
Rb
EN
CLa
Ra
EN
CLb
clk.a
108
clk.b
106
102
104
134
LDR.b
122
LDR.a
120
good.a
D Q
gooddel.a
clk.a
good.b
D Q
gooddel.b
clk.b
LDR.a = good.b or not(gooddel.a)
LDR.b = good.a or not(gooddel.b)
clk.a
CLOCK CONTROL LOGIC
clk.b
sysclk

FIG. 6

URI.5077

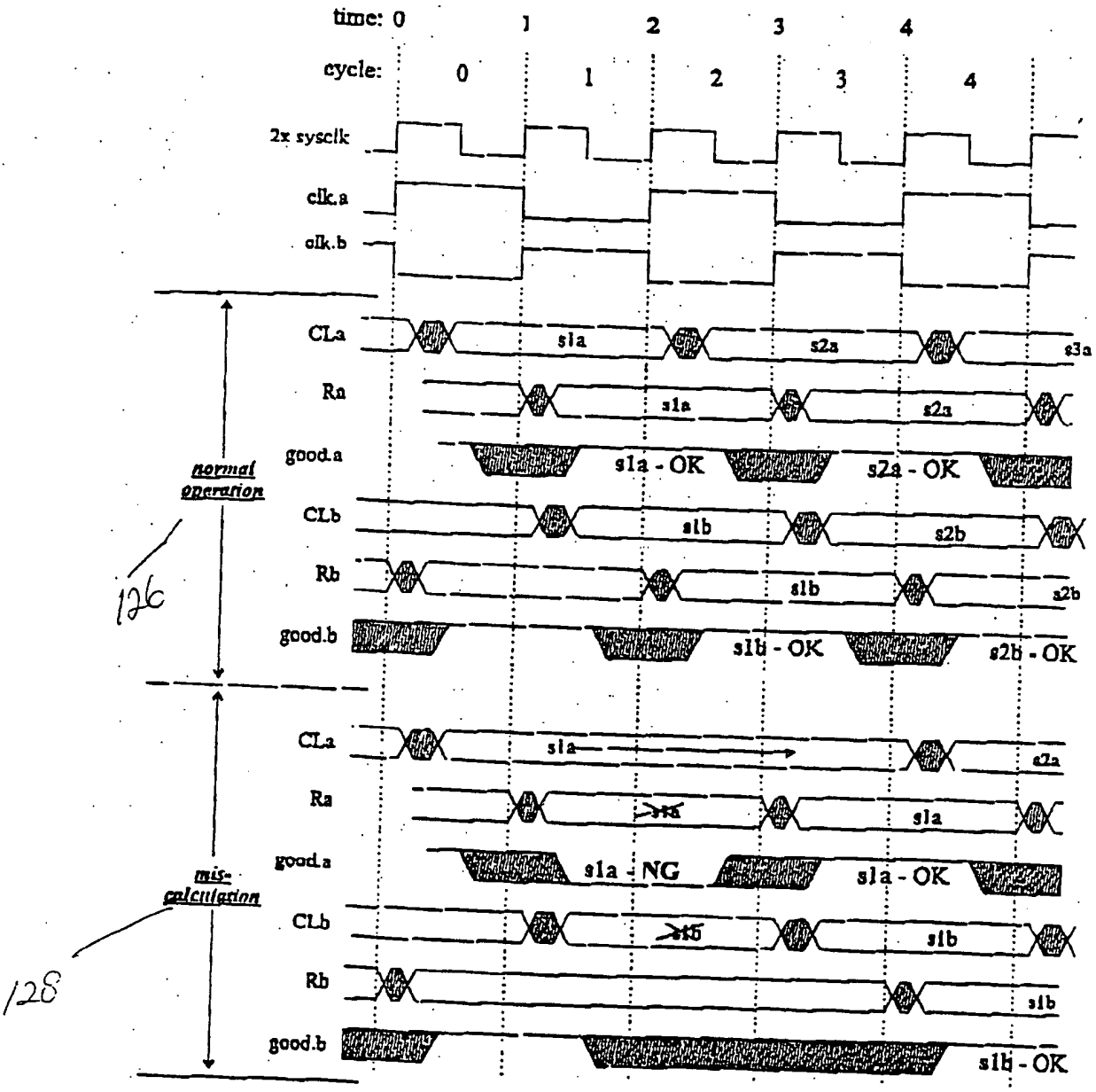


FIG. 7

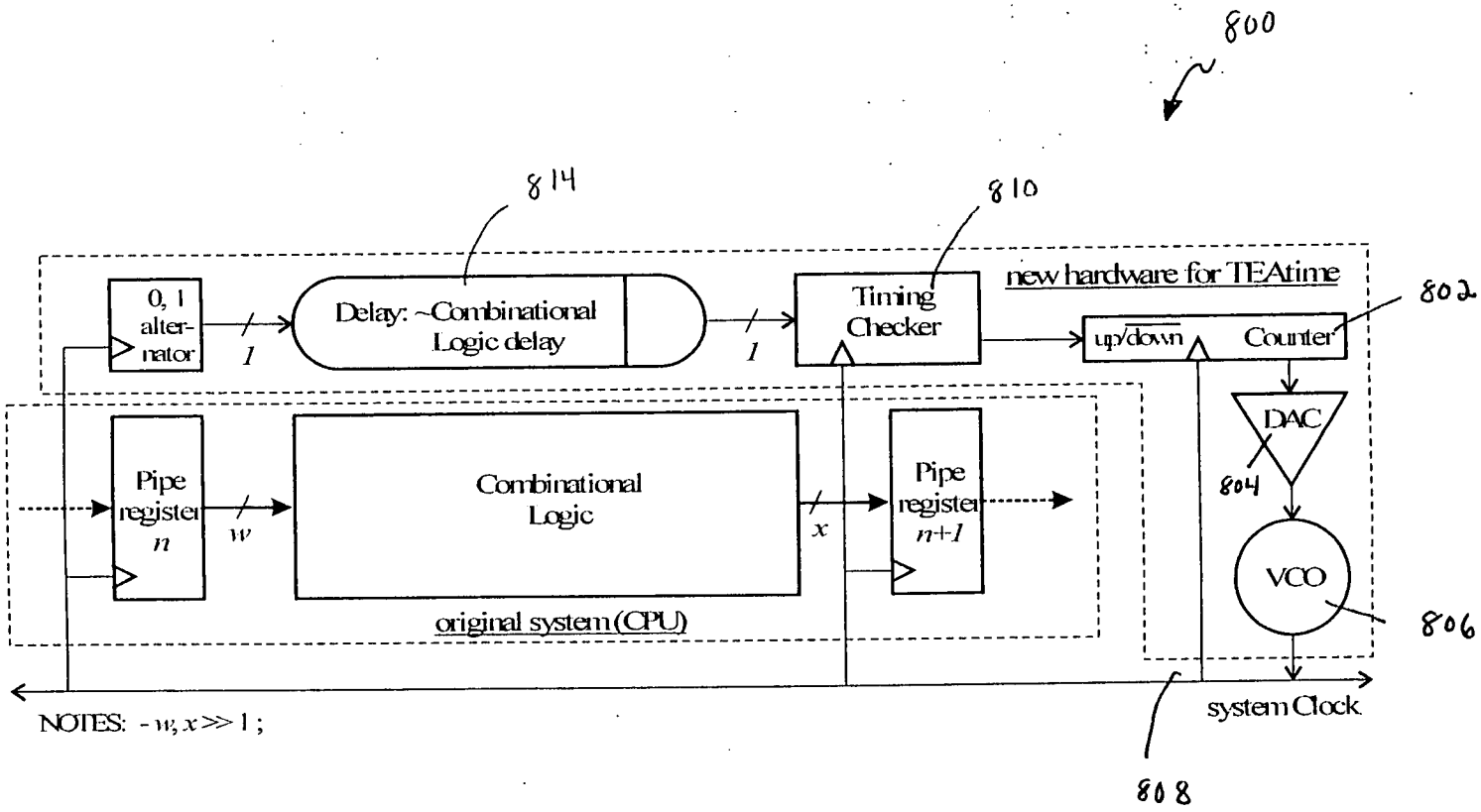

800
814
810
new hardware for TEAtime
802
0, 1 alter-nator
1
Delay: ~Combinational Logic delay
1
Timing Checker
up/down
Counter
DAC
804
Pipe register n
w
Combinational Logic
x
Pipe register n+1
VCO
806
original system (CPU)
NOTES: - w, x >> 1 ;
system Clock
808

FIG. 8

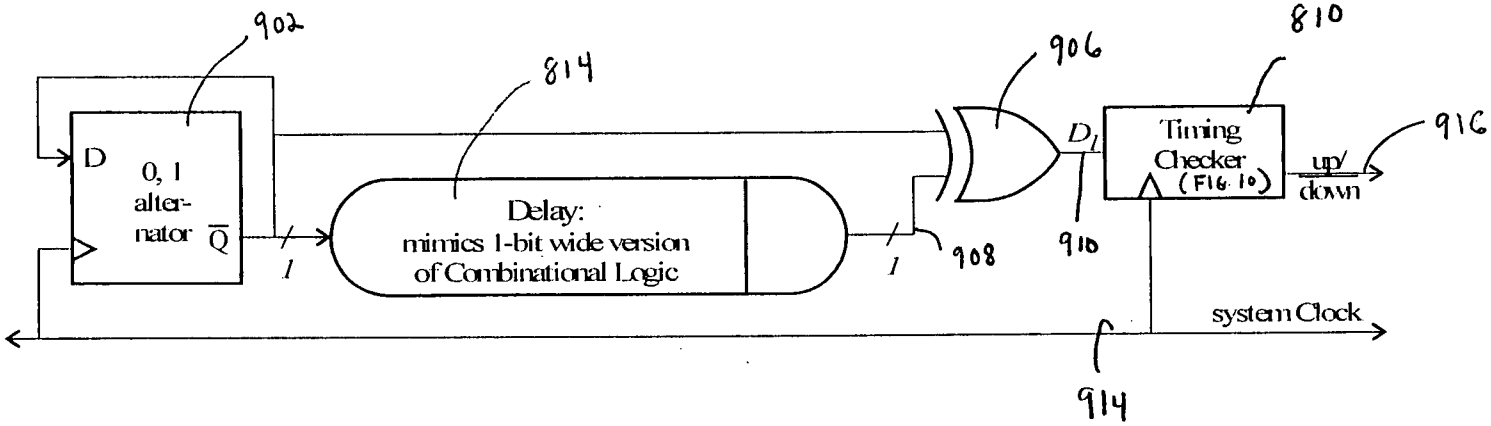

902
814
906
810
D
0, 1
alter-
nator
$\overline{Q}$
1
Delay:
mimics 1-bit wide version
of Combinational Logic
1
908
D_1
910
Timing
Checker
(FIG. 10)
up/
down
916
system Clock
914

FIG. 9

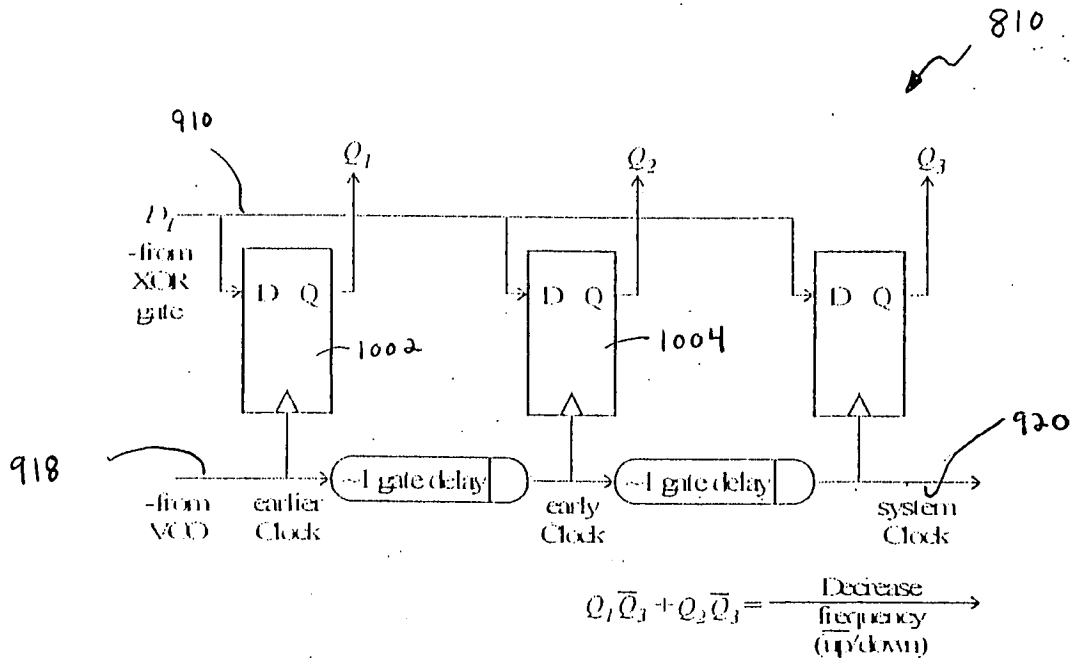

810
910
Q_1
Q_2
Q_3
D_1
-from XOR gate
D Q
D Q
D Q
1002
1004
920
918
-from VCO
earlier Clock
1 gate delay
1 gate delay
early Clock
system Clock
$Q_1\overline{Q}_3 + Q_2\overline{Q}_3 =$
Decrease frequency (up/down)

FIG. 10

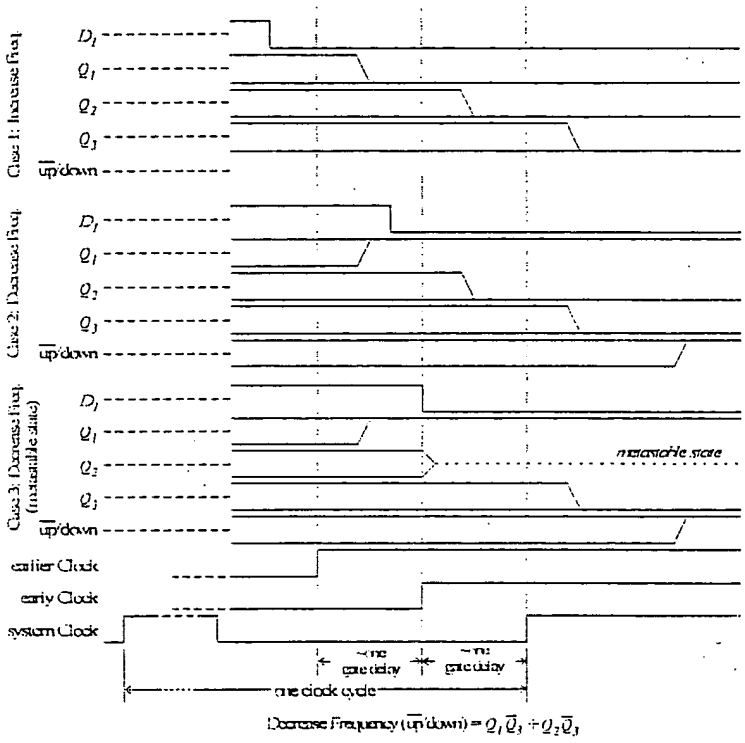

Case 1: Increase Freq
Case 2: Decrease Freq
Case 3: Decrease Freq (metastable state)
D_1
Q_1
Q_2
Q_3
$\overline{up/down}$
metastable state
earlier Clock
early Clock
system Clock
one gate delay
one gate delay
one clock cycle
Decrease Frequency ($\overline{up/down}$) = $Q_1\overline{Q}_3 + Q_2\overline{Q}_3$

FIG. 11